REMARKS

Claims 1 and 2 were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. On page 5, lines 32-33, and page 6, lines 1-10 the idea of same voltage is clearly defined. In the above referenced portion of the disclosure the gate, drain, and source terminals of the NMOS and PMOS transistors are clearly defined and shown in Figure 3. The text describes where in the circuit the same voltages should be applied and the resulting current. This is within the requirements of 35 USC 112 as it pertains to the required description of the invention. The examiners rejection is therefore unfounded.

Claims 1 and 2 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as their invention. The antecedent basis is in the above-described sections of the disclosure. The examiners rejection is therefore unfounded.

Claims 1 and 2 were rejected under 35 U.S.C. 102(e) as being anticipated by Leung. Claim 1 has been amended to include the limitation of "during a read operation a voltage applied to the word line is less than 90% of the supply voltage." The examiner states that during a read operation, the voltage applied to the word line WL is less than the supply voltage Vcc by a threshold voltage of the PMOS transistor. This is an incorrect statement. The voltage applied to the word line is independent of the threshold voltage of the PMOS transistor. From Figure 5, the word line voltage is applied to the gate of the NMOS transistor. The drain of the various transistors has nothing to do with the voltage that is applied to word line and therefore to the gate of the NMOS transistors. In light of the current understanding of MOS transistor circuit theory the examiners statement has little meaning. Amended claim 1 is allowable over the cited art.

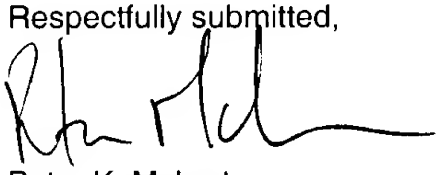
In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made."**

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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Version with Markings to Show Changes Made

1(Amended). A memory cell, comprising:

providing a PMOS drive transistor with a gate terminal, a first source/drain terminal, and a second source/drain terminal;

providing a NMOS pass transistor with a gate terminal, a first source/drain terminal and a second source/drain terminal;

connecting said first source/drain terminal of said NMOS pass transistor to a bitline;

connecting said second source/drain terminal of said NMOS pass transistor to a first storage node;

connecting said gate terminal of said NMOS pass transistor to a wordline;

connecting said first source/drain terminal of said PMOS drive transistor to a supply voltage;

connecting said second source/drain terminal of said PMOS drive transistor to said first storage node;

connecting said gate terminal of said PMOS drive transistor to a second storage node; and

wherein a current flowing through the source/drain terminals of the NMOS pass transistor is greater than a current flowing through the source/drain terminals of the PMOS drive transistor for the same voltages applied between the gate and source/drain terminals of the PMOS drive transistor and the gate and source/drain terminals of the

NMOS pass transistor and during a read operation a voltage applied to the wordline is less than 90% of the supply voltage.